QUALIFICATION FILE: Advanced Diploma –VLSI Physical Design Engineer (Level 7)

NSDA REFERENCE
To be added by NSDA

QUALIFICATION FILE – CONTACT DETAILS OF SUBMITTING BODY

Name and address of submitting body:

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT),
NIT CAMPUS POST,
CALICUT, KERALA.
PIN – 673601.

Name and contact details of individual dealing with the submission

Name:	Sreejeesh SG
Designation:	Technical Officer
Mobile:	9447769756
Email:	sreejeesh@nielit.gov.in, sree@calicut.nielit.in

List of documents submitted in support of the Qualifications File

a) Annexure I– Course Curriculum
b) Annexure II – Industry Validation
c) Annexure III : Occupational Map as identified by SSC mapped to Jobroles.
d) Evidence of job market / Industry requirement – Attached in Section3

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SUMMARY

Qualification Title:	Advanced Diploma –VLSI Physical Design Engineer
Qualification Code	
Nature and purpose of the qualification:	The purpose of this qualification is to train the students to be ready for Physical Design Engineer
Body /bodies which will award the qualification:	National Institute of Electronics and Information Technology 6-CGO Complex, Electronics Niketan Lodhi Road, New Delhi. 110003.
Body which will accredit providers to offer courses leading to the qualification:	National Institute of Electronics and Information Technology 6-CGO Complex, Electronics Niketan Lodhi Road, New Delhi. 110003.
Body /bodies which will Be responsible for assessment:	**Examination Cell,** National Institute of Electronics and Information Technology 6-CGO Complex, Electronics Niketan Lodhi Road, New Delhi. 110003.
Occupation(s) to which the qualification gives access:	Physical Design Engineer
Licensing Requirements	Not applicable
Proposed level of the qualification in the NSQF	Level 7
Anticipated volume of training/learning required to complete the qualification	480 Hours
Entry requirements/ Recommendations	B.Tech pursuing/ M.Sc pursuing in Electrical/ Electronics and Electronics and Instrumentation/ Computer Science and allied branches **Prerequisites**: Knowledge in Digital Design

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Progression from the Qualification	**Professional:** Physical Design Engineer->Senior Physical Design Engineer -> Principal Physical Design Engineer **Academic:** M.Tech in VLSI / Embedded System Design / Electronics System Design → Integrated PhD involving application research.
Planned arrangements for RPL.	Presently only candidates who undergo training shall be assessed. It will be incorporated once RPL strategy is finalized
International Compatibility where Known.	Not Known Yet
Date of Planned review of the Qualification	After Every 2 Years

Formal Structure of the Qualification			
Title ofComponent and Identification Code	**Mandatory/ Optional**	**Estimated Size** (Learning hours)	**Level**
Introduction to IC Design Flow	M	40	7
Basic CMOS Digital IC Design	M	80	7
Processing and Layout	M	80	7
System Design and Design Methods	M	80	7
Analog IC Design	M	80	7
Project	M	120	7

Detailed Curriculum attached as – **Annexure I**

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SECTION –1

ASSESSMENT

Name of Assessment body:

Examination Cell,
National Institute of Electronics and Information Technology
6-CGO Complex, Electronics Niketan
Lodhi Road, New Delhi. 110003.

Name of body checking or verifying Assessments:

Examination Cell,
National Institute of Electronics and Information Technology
6-CGO Complex, Electronics Niketan
Lodhi Road, New Delhi. 110003.

Name of Qualification Awarding body:

National Institute of Electronics and Information Technology.

Will the assessment body be responsible for the RPL assessment?

RPL Policy will be described as and when available

Describe the overall assessment strategy and specific arrangements which have been put in place to ensure that assessment is always valid, consistent and fair and show that these are in line with the requirements of NSQF:

This course would lay more emphasis on developing the practical skills of the student. His overall knowledge shall be tested based on a comprehensive written assessment, his practical skills shall be equally measured with a detailed practical assessment. The communication/technical skills of the student and his ability to express himself shall be tested in Viva Voce Assessment. Each assessment shall define an OUTCOME and marked separately. Student shall be required to pass in all OUTCOMEs individually and marks shall be allotted for each OUTCOME along with final aggregate marks in course.

Following assessment methodologies may be used:

A. Written Assessment

B. Practical Assessment

C. Viva Voce Assessment

Supporting evidences for Assessment

The assessment results are backed by following evidences.

1. The assessor collects a copy of the attendance for the training done under the scheme. The attendance sheets are signed and stamped by the In charge / Head of the Training Centre.

2. The assessor verifies the authenticity of the candidate by checking the photo ID card issued by the institute as well as any one Photo ID card issued by the Central/Government. The same is mentioned in the attendance sheet

ASSESSMENT EVIDENCE

Job Role: Physical Design Engineer

Title of Unit/Component: Advanced Diploma –VLSI Physical Design Engineer

Outcomes to be assessed	Assessment Criteria for the outcome	Means of Assessment			
		Total Marks	Written	Practical	Project
Concepts of IC Design Flow, Verilog RTL Coding skills	Design Digital circuit from specification. Demonstrate the digital circuit in Verilog RTL model, test and validate the circuit Use Mentor Graphics Modelsim, Xilinx ISE, Cadence Environment VLSI CAD Tools to demonstrate Verilog RTL modelling and testing of	50	25	25	NA

	digital circuit. State Linux/Windows Operating System.				
CMOS Logic Design skills RTL to GDSII flow mechanism.	Demonstrate mathematically the CMOS inverter transfer characteristics, by varying W/L ratio of inverter. Use ASIC backend tools from CADENCE/Synposys to demonstrate the CMOS inverter transfer characteristics. Generate GDSII file of a complex digital circuit.(RISC CPU) Explain DRC,LVS, CTS, ERC and antenna checks. Use of ASIC Backend tools for the same. Design Complex CMOS circuits based on pass transistor, transmission gates and inverters. Static Timing Analysis.	50	25	25	NA
Learn various parameters & characteristics of CMOS & CMOS fabrication flow	Extracting various CMOS mask layers. Explain Process parameterization, CMOS Circuit Characterization estimating Speed, Power and circuit area.	50	25	25	Na

	Compare CMOS fabrication flow.				
Analog IC Design skills for industry standard designs	Design CMOS OPAMP and demonstrate the performance using CADENCE Spectra Tool. Explain about Transistor layout, Capacitor Matching, Resistance layout. Explain DRC,LVS and Antenna checks of Analog Layout. Design Complex Analog circuit like Instrumentation Amplifier.	50	25	25	Na
VLSI Backend Design skills.	Perform Floor planning, power planning, Placement, clock tree synthesis and Routing of Gate level netlist. Physical Verification and DFM Checks Signal integrity and back annotation Sign off Checks and Tape out/Handoff	100			100
	Grand Total	300			

Pass/Fail

Following Grading Scheme (on the basis of total marks) will be followed:

Grade	S	A	B	C	D	E	Fail
Marks Range (in %)	≥90%	80%–89%	70%–79%	60%–69%	50%–59%	40–49%	<40%

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SECTION 2

EVIDENCE OF LEVEL

Title: Advanced Diploma –VLSI Physical Design			Level : 7
NSQF Domain	**Outcomes of the Qualification/Component**	**How the job role relates to the NSQF Level Descriptors**	**NSQF Level**
Process required	Specification to GDSII file generation process. This includes VLSI Frontend and backend design process. Candidate will acquire comprehensive knowledge in above process.	Demands a wide range of specialised technical skill, clarity of knowledge and practice in broad range of activity involving standard and non-standard VLSI Design practices.	7
Professional knowledge	Factual and theoretical knowledge about Backend ASIC design Flow (Netlist to GDSII) such as; CTS, DRC, LVS, antenna checks, ERC, IOPAD layout, placement and routing concepts and proficiency in CADENCE IC back end design tools	Factual and theoretical knowledge in broad contexts within a field of VLSI Physical design.	7
Professional skill	Candidate will acquire theoretical and practical problem solving skill in the field of Physical Design of Digital and Analog Circuits and Systems.	A range of cognitive and practical skills required to generate solutions to specific problems in VLSI Physical design a field.	7

Core skill	Candidate will be good in Digital Logic Design, mathematical skills, will be able to understand the practical requirements and will be able to effectively communicate and deliver the solutions by collecting data and passing information in an effective manner.	Reasonable good in mathematical calculation, understanding of social, political and reasonably good in data collecting organising information, and logical communication.	7
Responsibility	Candidate will be able to work independently with responsibility in the ASIC Physical Design industry; he/she also can supervise others work and help them learn.	Responsibility for own work and learning and full responsibility for other's works and learning.	7

SECTION 3

EVIDENCE OF NEED

What evidence is there that the qualification is needed?

To facilitate skill development in ESDM sector focusing on students/unemployed youth at 9-10th standard onwards, ITI, Diploma, Non-engineering graduates, etc. to increase their employability to work in '**Manufacturing**' and '**Service support**' functions, a '**Scheme for Financial Assistance to select States/UTs for Skill Development in Electronics System Design and Manufacturing (ESDM) sector**' was approved by Department of Electronics and Information Technology (DeitY), Ministry of Communication& Information Technology, Govt. of India on 1st November, 2013.

1. Report of taskforce to suggest measures to stimulate the growth of IT, ITES, and Electronics Hardware manufacturing Industry in India – Dec 2009.

RECOMMENDATIONS

The Government of India would do well to foster a globally competitive industry.

The industry needs to focus on the following:

- Increased value addition
- Implementation of best practices
- Catering to the needs of domestic and global markets by creating innovative product designs and R&D
- Driving cost competitiveness

The government can catalyze this growth by the following measures:

1	Establish 'National Electronics Mission'	Establish 'National Electronics Mission' – a nodal agency for the electronics industry within DIT and with direct interface to the Prime Minister's Office (PMO). The nodal agency will help in the synchronized functioning of the industry. It will enhance the ease of doing business.
2	Promote existing clusters and create new ones	Create islands of excellence by encouraging and planning for the expansion of existing centers such as Sriprembudur, Noida, etc. and identify more locations to set up clusters to create a complete ecosystem where all the segments of the value chain are available at one location. Provide contiguous land and Infrastructure to the industry to these clusters.
3	"Made for India" Goods	Encourage products specifically designed for India. Developmental sector can benefit from biometric readers, smart meters, micro payment devices, and low cost devices.
4	Creation of a R&D fund	A fund may be created to incentivize R&D, where the government and the industry bodies are stake holders.
5	Creation of a manufacturing value addition fund	A separate fund may also be created to provide interest linked subsidy to promote value added manufacturing and create products for India.
6	Rationalization of tax structure	Stable tax structure needs to be put in place in order to encourage long term investment by the companies.
7	Promote skill development	Government needs to focus on skill development, regulations around over-time and contracts need to be flexed.

2. Challenges and Solutions in bridging the gap of skilled human Resource (HR) in Electronics System Design and Manufacturing System. Workshop report Feb 2012.

3. Proposal to NSDC on the formation of Sector Skills Council: Electronics.

4. Employability and skills set of newly graduated Engineers in India – Andreas Blom, Hiroshi Sakei policy research working paper (5640). World Bank.
5. Human Resource and skill Requirements in the Electronics and IT Hardware Industry. "Study on mapping of human resource Skill gaps in India till 2022" – NSDC / ICRA management Consulting Services Limited. (IMACS).

   https://www.scribd.com/document/74364619/Media-Entertainment-Human-Resource-Skill-Gaps-India-2012
6. *View Point* – Make in India – *"A Way to Boost Manufacturing and Employment opportunities" Electronics for You, June 2016.*

Evidence of qualification Requirement in the Industry – There is huge opportunities for Physical Design Professionals in the industry – proof from Naukari.com, LinkedIn attached. The job Title showsthat it is directly linked with our contents.

1. Job details from linkedin.com

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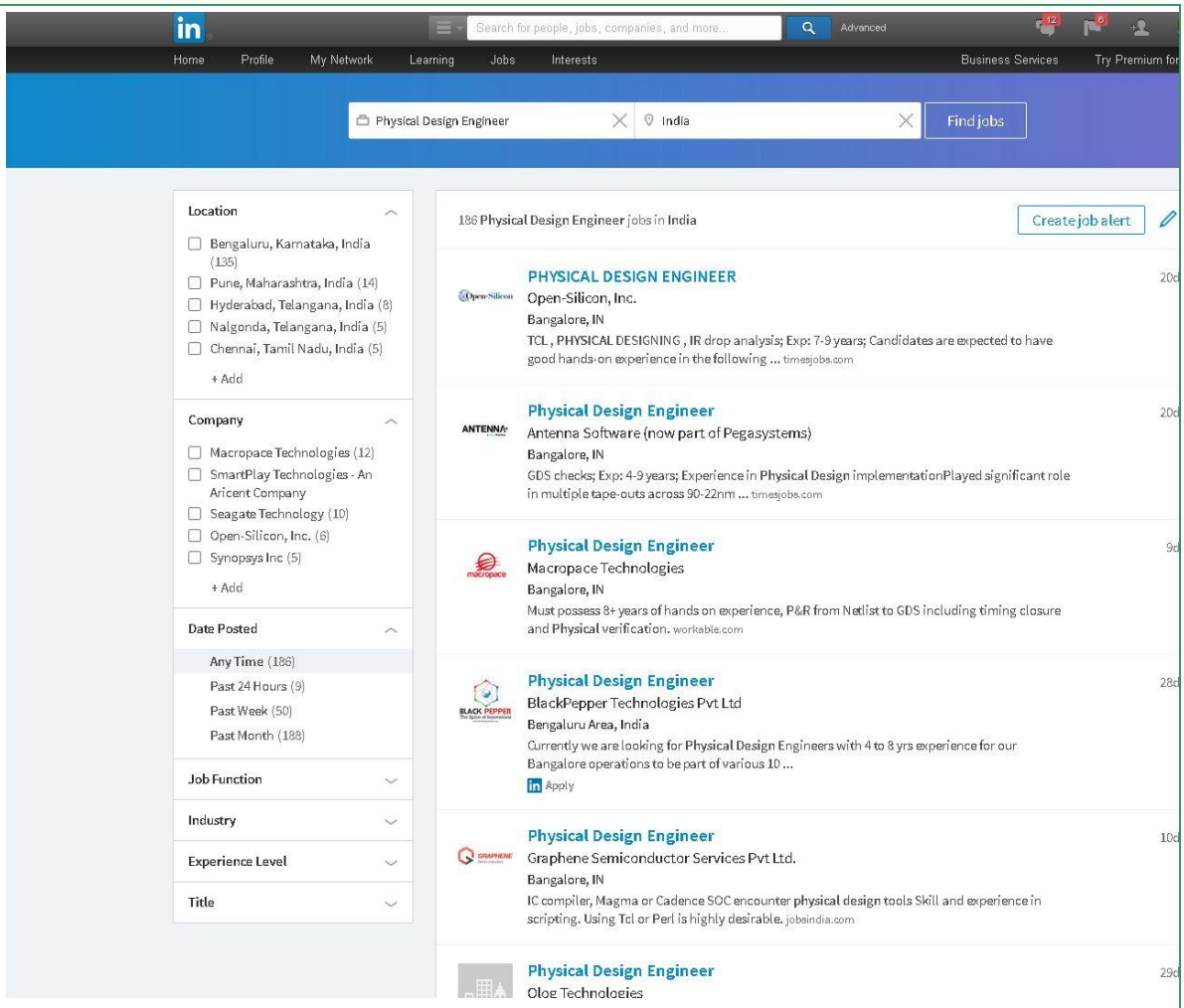

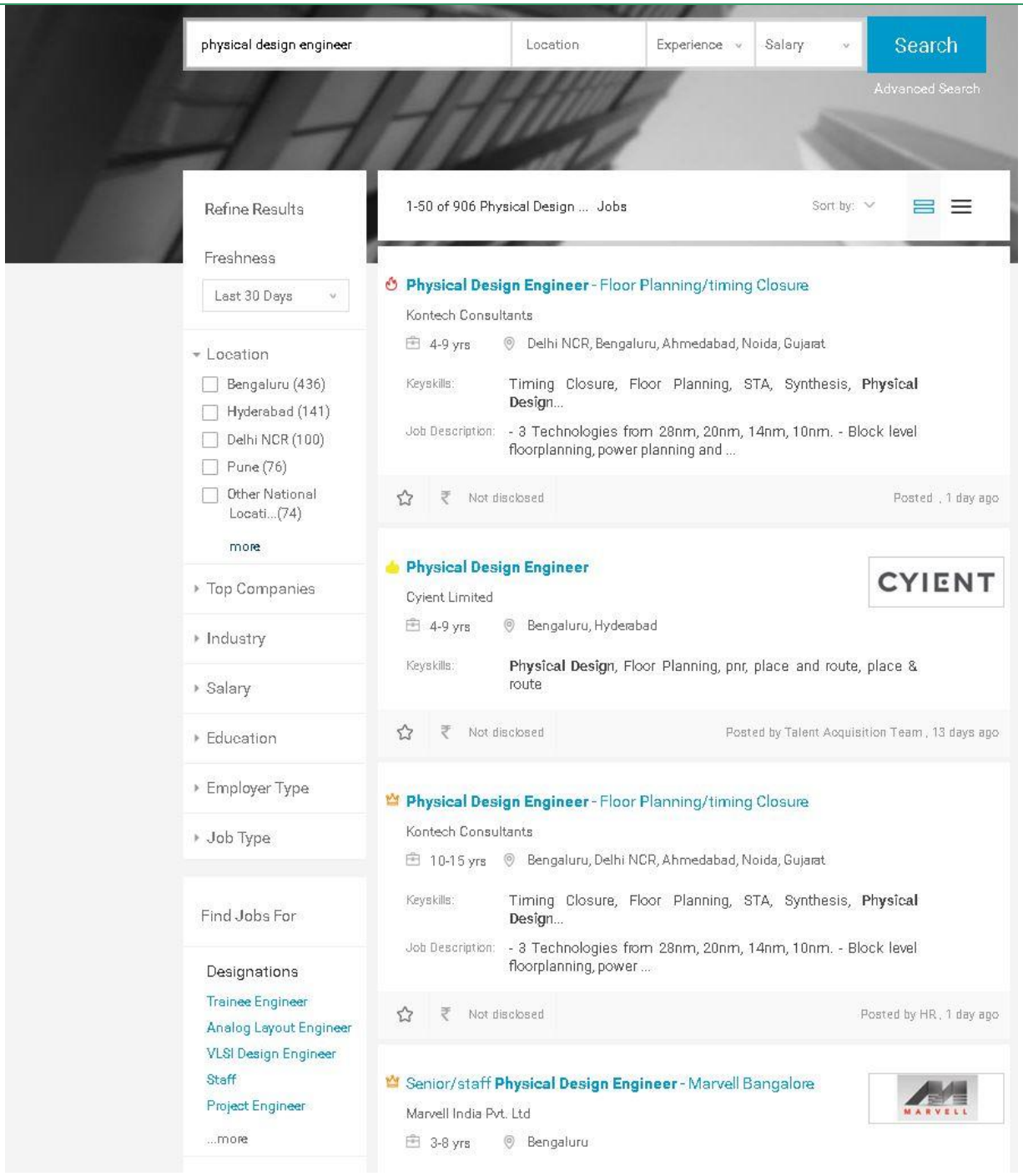

What is the estimated uptake of this qualification and what is the basis of this estimate?

Estimated uptake is 15 students / Batch with 2 Batches / Year and on the basis of market Survey /other reports and our infrastructure capabilities.

There is huge opportunities for Physical Design Professionals in the industry – proof from

Naukari.com, LinkedIn attached.
What steps were taken to ensure that the qualification(s) does/do not duplicate already existing or planned qualifications in the NSQF? No courses as per our knowledge aligned to the standards.
What arrangements are in place to monitor and review the qualification(s)? What data will be used and at what point will the qualification(s) be revised or updated?
After each course, a course feedback will be collected from completed students which will be reviewed by a committee and ratifications will be applied. Based on feedback by participants, employers and based on market survey the qualification will be reviewed in every 2 years.Feedbacks of each trainee are used by core committee for revision and up gradation of the qualification. The curriculum review and updates, in consultation with industries and expert of respective domain, NOS approved by NSDA will also be referred from time to time.

SECTION 4

EVIDENCE OF PROGRESSION

What steps have been taken in the design of this or other qualifications to ensure that there is a clear path to other qualifications in this sector? This course structure is designed in such a way that, the qualification acquired will meet the prerequisites of higher level courses in this domain like MTech in VLSI, Embedded System Design, Electronics System Design and Integrated PhD involving application research.

SECTION 5
EVIDENCE OF INTERNATIONAL COMPARABILITY

List any Comparisons which have been established – NIL