QUALIFICATION FILE: Certificate Course in VLSI Design (Level 05)

NSDA Reference
To be added by NSDA

Revised Application Documentation:

QUALIFICATION FILE – CONTACT DETAILS OF SUBMITTING BODY

Name and address of submitting body:

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT), CALICUT
NIT CAMPUS POST, KOZHIKODE, KERALA.
PIN – 673601.

Name and contact details of individual dealing with the submission:

Name: Nandakumar R

Designation: Scientist/ Engineer 'C'

Mobile: 9995427802

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List of documents submitted in support of the Qualifications Files(attached)

1. Annexure I - Course Curriculum
2. Annexure II – Industry Validation
3. Annexure III - Occupational Map as identified by SSC mapped to Jobroles.
4. Evidence of Job Market / Requirement in the Industry (included in section 3)

QUALIFICATION FILE: Certificate Course in VLSI Design (Level 05)

SUMMARY

Qualification Title:

- Certificate course in VLSI Design

Qualification Code

Nature and purpose of the Qualification:

- This Qualification is aligned to Level 05.
- The purpose of this qualification is to train the students to be ready for RTL Design Engineering Job.

Body/bodies which will award the qualification:

National Institute of Electronics and Information Technology
6-CGO Complex, Electronics Niketan
Lodhi Road, New Delhi. 110003.

Body which will accredit providers to offer courses leading to the qualification:

National Institute of Electronics and Information Technology
6-CGO Complex, Electronics Niketan
Lodhi Road, New Delhi. 110003.

Body/bodies which will be responsible for assessment:

Examination Cell,
National Institute of Electronics and Information Technology
6-CGO Complex, Electronics Niketan
Lodhi Road, New Delhi. 110003

Occupation(s) to which the qualification gives access:

RTL Design Engineer

Licensing Requirements: Not applicable

Proposed level of the qualification in the NSQF:

Level 05

Anticipated volume of training/learning required to complete the qualification:

80 Hours

Entry requirements / recommendations:

- Pursuing Engineering Degree [ECE/EEE/CSE/AEI]

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Progression from the qualification:

Professional: RTL Engineer > Sr. RTL Engineer
Academic :Advance Diploma in VLSI physical Design Engineer(level 7)-> PG Diploma in VLSI and Embedded hardware Design (Level 8)

Planned arrangements for the Recognition of Prior learning (RPL):

- Presently only candidates who undergo training shall be assessed.
- It will be incorporated once RPL strategy is finalized

International comparability where known: NA

Formal structure of the qualification:

Course Structure:

This course contains total three modules.

S.no	***Module***	***Mandatory /Optional***	***Estimated Size (Hours)***	***Level***
1	*Advanced Digital Design Review*	*Mandatory*	*12*	*5*
2	*Hardware Description Language (Verilog HDL)*	*Mandatory*	*40*	*5*
3	*FPGA Architecture and Prototyping*	*Mandatory*	*28*	*5*

1: *Advanced Digital Design Review*

Duration: 12 Hours

Description

- Combinational Circuit Design
- Sequential Circuit Design
- Design of controller and Data path units
- State Machines
- Controller Design using FSMs & ASMs
- Design Examples & Case Studies

2: Hardware Description Language (Verilog HDL)

Duration: 40 Hours

Description

- Introduction to Verilog HDL & Hierarchical Modeling Concepts
- Lexical Conventions & Data Types

- System Tasks & Compiler Directives
- Modules, Ports and Module Instantiation Methods
- Modeling methods.
- Design Verification using Test benches

3: FPGA Architecture and Prototyping

Duration: 28 Hours

Description

- Introduction to Programmable Logic and FPGAs
- Popular CPLD & FPGA Families
- Architecture of popular Xilinx and Altera FPGAs
- FPGA Design Flow
- Implementation Details
- Advanced FPGA Design tips
- Logic Synthesis for FPGA
- Design problems(Mini Project)

SECTION 1

ASSESSMENT

Body/Bodies which will carry out assessment:

Examination cell
National Institute of Electronics and Information Technology
6-CGO Complex, Electronics Niketan
Lodhi Road, New Delhi. 110003

Will the assessment body be responsible for RPL assessment?

RPL Policy will be described as and when available

Describe the overall assessment strategy and specific arrangements which have been put in place to ensure that assessment is always valid, consistent and fair and show that these are in line with the requirements of the NSQF:

Assessment is done by
Examination cell
National Institute of Electronics and Information Technology
6-CGO Complex, Electronics Niketan, Lodhi Road, New Delhi. 110003

The assessment strategy is unique to each module which bifurcate the theory and practical with higher emphasis on Practical Assessment.

The assessment consists of

ii) Theory (Module 1) - 50 Marks
iii) Practical (Module 2) - 50 Marks
iv) Practical (Module 3) - 50 Marks
v) Mini – Project / Case Study - 100 Marks
Total -250 Marks

During conduction of the course, the internal marks are awarded based on the Progress of Lab Exercises and Attendance. Theory /Practical Examination are conducted at the end of each module. A mini project work is evaluated with oral presentation and live demo of project. Case study is monitored by their analysis and oral presentation of particular topics.

ASSESSMENT EVIDENCE

Outcomes to be assessed	**Assessment Criteria for the outcome**	**Means of Assessment**			
		Total Marks	**Written**	**Practical**	**Project**
Designing of Digital Circuit	1.Designing of Combinational Circuit adder, Substractor, MUX, DEMUX, Encoder and Decoder. 2 Design Sequential Circuit: Flip flop and Counter. 3 Develop FSMs & ASMs for the given problems.	50	50	NA	NA
Analyze Verilog HDL Coding Logic Design and Synthesis	1 Write Verilog code, compile, simulate and execute on any VLSI design platform. 2 Perform verification and testing	50	NA	50	NA
FPGA prototyping	1 Apply Verilog HDL for FPGA Programming 2 Implement Digital Circuits	150	NA	50	100

	on Xilinx FPGAs and Altera FPGAs using Verilog HDL				
	Grand Total	250	50	100	100

Module wise assessment is conducted after the end of the each module. For assessing whether the candidate has learned the concepts properly, a theory examination is conducted with multiple choice questions (MCQ). For assessing the practical skills acquired, a practical examination is conducted, where the student has to solve a given problem, code, simulate, verify, synthesize and prototype on the required hardware and software platforms.

Module1

- For assessing whether the participant can apply the learned concept of combinational and sequential digital design, a theory examination is conducted with multiple choice questions.
- For assessing whether the participant can apply the learned concept of State Machine,a oral presentation is conducted for 20 minutes by each student where the student has to explain the flow of path from one state to another using state diagram and state table.
- For assessing whether the participant can apply the learned concept of FSM and ASM, a mini – project is implemented.

Module2

- For assessing whether the participant can apply the learned concept of Logic and synthesis design, Verilog HDL programming, a Practical Examination is conducted for 3 hours duration where the student has to solve a problem, code it in Verilog, compile, simulate and execute in Design suites from Mentor Graphics® / Cadence® /Synopsys® etc

Module3

- For assessing whether the participant can apply Verilog HDL Programming and Implementation of Verilog HDL Code on Xilinx FPGA, a Practical Examination is conducted where the student has to solve a problem, code it and port on FPGAs using Xilinx ISE and Altera FPGA Design Suite (Quartus).

Grade	**S**	**A**	**B**	**C**	**D**	**E**	**Fail**
Marks Range (in %)	≥90%	80%-89%	70%-79%	60%-69%	50%-59%	40-49%	<40%

SECTION 2

EVIDENCE OF LEVEL

Title : Certificate Course in VLSI Design			**Level : 5**
NSQF Domain	**Outcomes of the Qualification/Component**	**How the job role relates to the NSQF Level Descriptors**	**NSQF Level**
Process required	The candidate is required to apply the Advanced digital design concepts, Verilog HDL coding skills and FPGA based prototyping skills for translation of specification to RTL Design and FPGA prototyping	Job that requires well developed skill, with clear choice of procedures in familiar context.	**5**
Professional knowledge	Factual knowledge about:- Terminologies associated with Digital design, HDL & FPGA prototyping. Elements Melay & More FSMs, ASMs, data path control path, lexical conventions, mega plug in wizards, processor cores etc.	Knowledge of facts, A principles, processes and general concepts, in a field of work or study.	**5**
Professional skill	Verilog HDL Coding Skills and FPGA based Prototyping Skills for translation of specification to RTL Design and FPGA prototyping	A range of cognitive and practical skills required to accomplish tasks and solve problems by selecting and applying basic methods, tools, materials and information	**5**
Core skill	Language to communicate with written or oral, with required clarity , skill to basic arithmetic and algebraic principles, basic understanding of social, political and natural environment	Desired mathematical skill; understanding of social, political; and some skill of collecting and organizing information, communication.	**5**
Responsibility	Candidate will be able to work independently in front end VLSI with responsibility required and he can guide the works of his team members	Responsibility for own work and learning and some responsibility to other's works and learning.	**5**

SECTION 3

EVIDENCE OF NEED

What evidence is there that the qualification is needed?

1. Report of taskforce to suggest measures to stimulate the growth of IT, ITES, and Electronics Hardware manufacturing Industry in India – Dec 2009.

RECOMMENDATIONS

The Government of India would do well to foster a globally competitive industry.

The industry needs to focus on the following:

- Increased value addition
- Implementation of best practices
- Catering to the needs of domestic and global markets by creating innovative product designs and R&D
- Driving cost competitiveness

The government can catalyze this growth by the following measures:

1	Establish 'National Electronics Mission'	Establish 'National Electronics Mission' – a nodal agency for the electronics industry within DIT and with direct interface to the Prime Minister's Office (PMO). The nodal agency will help in the synchronized functioning of the industry. It will enhance the ease of doing business.
2	Promote existing clusters and create new ones	Create islands of excellence by encouraging and planning for the expansion of existing centers such as Sriprembudur, Noida, etc. and identify more locations to set up clusters to create a complete ecosystem where all the segments of the value chain are available at one location. Provide contiguous land and Infrastructure to the industry to these clusters.
3	"Made for India" Goods	Encourage products specifically designed for India. Developmental sector can benefit from biometric readers, smart meters, micro payment devices, and low cost devices.
4	Creation of a R&D fund	A fund may be created to incentivize R&D, where the government and the industry bodies are stake holders.
5	Creation of a manufacturing value addition fund	A separate fund may also be created to provide interest linked subsidy to promote value added manufacturing and create products for India.
6	Rationalization of tax structure	Stable tax structure needs to be put in place in order to encourage long term investment by the companies.
7	Promote skill development	Government needs to focus on skill development, regulations around over-time and contracts need to be flexed.

2. Challenges and Solutions in bridging the gap of Skilled human Resource (HR) in Electronics System Design and Manufacturing System. Workshop report Feb 2012.
3. Proposal to NSDC on the formation of Sector Skills Council: Electronics.
4. Employability and skills set of newly graduated Engineers in India – Andreas Blom, Hiroshi Sakei policy research working paper (5640). World Bank.
5. Human Resource and skill Requirements in the Electronics and IT Hardware Industry.

"Study on mapping of human resource Skill gaps in India till 2022" – NSDC / ICRA management Consulting Services Limited. (IMACS)

https://www.scribd.com/document/74364619/Media-Entertainment-Human-Resource-Skill-Gaps-India-2012

6. *View Point* - Make in India - *"A Way to Boost Manufacturing and Employment opportunities" Electronics for You, June 2016.*

Job requirements involving the skills imparted through this program, as advertised by core companies in the field are listed below

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FPGA/Digital Hardware Engineer

Mitre Corporation - Bedford, MA 01730

Familiarity with good digital design practices including approaches to design, implementation, verification, testing, documentation, and debugging....

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Digital IC Design Engineer

Marvell - Santa Clara, CA

Require in depth RTL design and verification. Require basic DFT/ATE design experience. Require team and result oriented engineer....

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Digital Design Engineer

Cirrus Logic

Working knowledge of digital design flow from architecture, RTL design, verification, and synthesis. Work in a team environment to create and engineer digital...

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RTL Design-engineer/sr Engineer/lead Engineer

Aricent Technologies (H) Limited

Bengaluru, Chennai

Keyskills: System Verilog, Ahb, VHDL, **RTL**, Primetime, STA, Synthesis, SOC...

Job Description: Location: Bangalore, chennai A strong background in **RTL** level Digital ...

What is the estimated uptake of this qualification and what is the basis of this estimate?

Estimated uptake is 40 students / Batch with 2 Batches / Year and on the basis of identified skill gap in the following report

1. Human Resource and skill Requirements in the Electronics and IT Hardware Industry.

"Study on mapping of human resource Skill gaps in India till 2022" – NSDC / ICRA management Consulting Services Limited. (IMACS)
What steps were taken to ensure that the qualification(s) does/do not duplicate already existing or planned qualifications in the NSQF? The Qualification does not exist as per the information available in public domain.
What arrangements are in place to monitor and review the qualification(s)? What data will be used and at what point will the qualification(s) be revised or updated? Based on feedback by participants, employers and market survey the qualification will be reviewed, revised and updated in every 2 years.

SECTION 4

EVIDENCE OF RECOGNITION AND PROGRESSION
What steps have been taken in the design of this or other qualifications to ensure that there is a clear path to other qualifications in this sector?
This course structure is designed in such a way that, the qualification acquired will meet the prerequisites of higher level courses in VLSI. (PG Diploma in VLSI and Embedded hardware Design (Level 8))