# Qualification File: PG Diploma in VLSI & Embedded Hardware Design (Level 8)

| NSDA REFERENCE |
| --- |
| *To be added by NSDA* |

## QUALIFICATION FILE – CONTACT DETAILS OF SUBMITTING BODY

### Name and address of submitting body:

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT),
NIT CAMPUS POST,
CALICUT, KERALA.
PIN – 673601.

### Name and contact details of individual dealing with the submission


Name: Nandakumar R

Designation: Scientist/ Engineer 'C'

Mobile: 9995427802

Email: nanda@nielit.gov.in


### List of documents submitted in support of the Qualifications File

a) Annexure I– Course Curriculum
b) Annexure II – Candidates trained
c) Annexure III – Placement Details
d) Annexure IV – Industry Validation
e) Annexure V – Occupational Map identified by SSC– mapped to Jobroles.
f) Evidence of job market / Industry requirement – Attached in Section3

# Qualification File: PG Diploma in VLSI & Embedded Hardware Design (Level 8)

## SUMMARY

| | |
|---|---|
| **Qualification Title:** | PG Diploma in VLSI & Embedded Hardware Design |
| **Qualification Code** | |
| **Nature and purpose of the qualification:** | This Qualification is aligned to Level 8<br>The purpose of this qualification is to train the students to be ready for RTL Design Engineering Job. |
| **Body /bodies which will award the qualification:** | National Institute of Electronics and Information Technology<br>6-CGO Complex, Electronics Niketan<br>Lodhi Road, New Delhi. 110003. |
| **Body which will accredit providers to offer courses leading to the qualification:** | National Institute of Electronics and Information Technology<br>6-CGO Complex, Electronics Niketan<br>Lodhi Road, New Delhi. 110003. |
| **Body /bodies which will Be responsible for assessment:** | **Examination Cell,**<br>National Institute of Electronics and Information Technology<br>6-CGO Complex, Electronics Niketan<br>Lodhi Road, New Delhi. 110003. |
| **Occupation(s) to which the qualification gives access:** | RTL Design Engineer |
| **Licensing Requirements** | N/A |
| **Proposed level of the qualification in the NSQF** | Level 8 |
| **Anticipated volume of training/learning required to complete the qualification** | 840 Hours |
| **Entry requirements/ Recommendations** | B.E./B.Tech in Electronics/Electronics & Communication/Electrical/ Electrical and Electronics/Instrumentation/ Biomedical /Computer Science/IT.<br>MSc in Electronics/ Instrumentation/ Computer Science/Information Technology. |

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|---|---|
| **Progression from the Qualification** | **Professional :**<br><br>RTL Design Engineer->VLSI Design Engineer-> VLSI Design Team Lead-> VLSI Design Manager<br><br>**Academic:** MTech in VLSI / Embedded System Design /Electronics System Design → Integrated PhD involving application research. |
| **Planned arrangements for RPL.** | Presently only candidates who undergo training shall be assessed.<br>It will be incorporated once RPL strategy is finalized |
| **International Compatibility where Known.** | Not Known Yet |
| **Date of Planned review of the Qualification** | After Every 2 Years |

**Formal Structure of the Qualification**

This course contains total eight modules. After completing the first seven modules, the students have to do a six weeks project using any of the topics studied to earn the PG Diploma

| Title of Component and Identification Code | Mandatory/ Optional | Estimated Size (Learning hours) | Level |
|---|---|---|---|
| Advanced Digital Design | M | *35* | *8* |
| VHDL : Language and Coding for Synthesis | M | *70* | *8* |
| Verilog HDL : Language and Coding for Synthesis | M | *105* | *8* |
| RTL Verification (System Verilog, UVM) | M | *175* | *8* |
| FPGA Design Methodology and Prototyping | M | *70* | *8* |
| CMOS Logic & Physical Design | M | *70* | *8* |
| Embedded Controller Based Product Design | M | *105* | *8* |

| | | | |
|---|---|---|---|
| Project Work | M | 210 | *8* |

Detailed Curriculum attached as – **Annexure I**

## SECTION -1

## ASSESSMENT

**Name of Assessment body:**

**Examination Cell,**
National Institute of Electronics and Information Technology
6-CGO Complex, Electronics Niketan
Lodhi Road, New Delhi. 110003.

**Name of body checking or verifying Assessments:**

**Examination Cell,**
National Institute of Electronics and Information Technology
6-CGO Complex, Electronics Niketan
Lodhi Road, New Delhi. 110003.

**Name of Qualification Awarding body:**

National Institute of Electronics and Information Technology.

**Will the assessment body be responsible for the RPL assessment?**

RPL Policy will be described as and when available

**Describe the overall assessment strategy and specific arrangements which have been put in place to ensure that assessment is always valid, consistent and fair and show that these are in line with the requirements of NSQF:**

This course would lay more emphasis on developing the practical skills of the student. His overall knowledge shall be tested based on a comprehensive written assessment, his practical skills shall be equally measured with a detailed practical assessment. The communication/technical skills of the student and his ability to express himself shall be tested in Viva Voce Assessment. Each assessment shall define an OUTCOME and marked separately. Student shall be required to pass in all OUTCOMEs individually and marks shall be allotted for each OUTCOME along with final aggregate marks in course.

Following assessment methodologies may be used:
A. Written Assessment
B. Practical Assessment
C. Viva Voce Assessment

**Supporting evidences for Assessment**

The assessment results are backed by following evidences.

1. The assessor collects a copy of the attendance for the training done under the scheme. The attendance sheets are signed and stamped by the In charge / Head of the Training Centre.
2. The assessor verifies the authenticity of the candidate by checking the photo ID card issued by the institute as well as any one Photo ID card issued by the Central/Government. The same is mentioned in the attendance sheet

## ASSESSMENT EVIDENCE

**Job Role:** RTL Design Engineer

**Title of Unit/Component:** PG Diploma in VLSI & Embedded Hardware Design

| Outcomes | Assessment Criteria for the outcome | Means of Assessment | | | |
|---|---|---|---|---|---|
| | | Total Marks | Written | Practical | Project |
| Design ability of combinational and sequential digital Circuits | Candidate shall be able to provide solutions involving<br>a) Combinational Circuit Design(Full & half Adder, Full & half Substractor, MUX, Encoder)<br>b) Sequential Circuit Design(Counter & Flip flop)<br>c) Develop FSMs & ASMs for the given problems | 50 | 50 | Na | Na |
| Logic designing, | Candidate shall be able to | 50 | Na | 50 | Na |

| | | | | | |
|---|---|---|---|---|---|
| synthesizing and VHDL programming | program in VHDL solutions involving<br>a) Write Verilog code, compile, simulate and execute on any VLSI DESIGN PLATFORM<br>b) Perform verification and testing | | | | |
| Verilog<br>HDL Programming, Logic design and synthesis. | Candidate shall be able to program in Verilog HDL solutions involving<br>a) Perform the verification and testing and simulating<br>b) Generate UVM for the Design functions<br>c) Test benching and Debugging of the functions | 50 | Na | 50 | Na |
| Programming in System Verilog, Object oriented programming for ASIC Design & Verification, UVM | Candidate shall be able to program in System Verilog HDVL solutions involving<br>a) Capturing Specification, Verification Plan, Compiling, Simulating, Test benching, Verification Plan<br>b) Generate UVM for the Design functions | 50 | Na | 50 | Na |
| FPGA based prototyping | Candidate shall be able to demonstrate using FPGA<br>a) Apply verilog HDL for FPGA Programming | 50 | Na | 50 | Na |

| | | | | | |
|---|---|---|---|---|---|
| | b) Implement Digital Circuits on Xilinx and Altera FPGAs using verilog HDL<br>c) Report Generation and Documentation | | | | |
| CMOS based Logic and Physical Design | Candidate shall be able to demonstrate knowledge in<br>a) Follow MOS Operating Principles<br>b) Design of Combinational Logic using MOS<br>c) Design of Sequential Logic using MOS<br>d) Physical Design using EDA Tool(s) | 50 | 50 | Na | Na |
| Product development ability | Candidate shall be able to demonstrate knowledge in<br>a)Apply product development process for realization of the product<br>b)Design and develop a standalone Embedded System using Microcontrollers through conceptual design, PCB Design, PCB Assembly, Testing, Integration etc. | 50 | 50 | Na | Na |
| Overall system integration in | Candidate shall be able to demonstrate knowledge | 250 | | | Yes |

| | | | | | |
|---|---|---|---|---|---|
| VLSI/Embedded Sector | in Electronic System Building | | | | |
| | **Grand Total** | 600 | | | |

**Pass/Fail**

Following Grading Scheme (on the basis of total marks) will be followed:

| **Grade** | **S** | **A** | **B** | **C** | **D** | **E** | **Fail** |
|---|---|---|---|---|---|---|---|
| **Marks Range (in %)** | ≥90% | 80%-89% | 70%-79% | 60%-69% | 50%-59% | 40-49% | <40% |

# Qualification File: PG Diploma in VLSI & Embedded Hardware Design (Level 8)

## SECTION 2

## EVIDENCE OF LEVEL

**Title/Name of qualification:** PG Diploma in VLSI & Embedded Hardware Design

<table>
<tr><td colspan="3">Title : P G Diploma in VLSI & Embedded Hardware Design</td><td>Level : 8</td></tr>
<tr><td>NSQF Domain</td><td>Outcomes of the Qualification/Component</td><td>How the job role relates to the NSQF Level Descriptors</td><td>NSQF Level</td></tr>
<tr><td>Process required</td><td rowspan="3">The candidate is required to apply the Advanced Digital Design Concepts, VHDL, Verilog HDL coding skills and FPGA based prototyping skills for translation of specification to RTL Design and FPGA prototyping.<br>They have to also apply their knowledge into the RTL Verification area also<br>Good Digital design and timing concepts, ASIC Flow, Full custom flow. IC fabrication techniques, Designing using Verilog, Verilog for verification, Exposure to Synthesis , Verification<br>Develop practical skills for implementing VLSI/Embedded strategies for Digital System Design projects. Will be able to solve the problems and will be effectively communicate.</td><td rowspan="3">The candidate is expected to posses Comprehensive, cognitive, theoretical knowledge and practical skills to develop creative solutions to abstract Problems<br>The candidate will be able to Undertake self-study; demonstrates intellectual independence, analytical rigour and good communication skills after undergoing the program</td><td>8</td></tr>
<tr><td>Professional knowledge</td><td>8</td></tr>
<tr><td>Professional skill</td><td>8</td></tr>
<tr><td>Core skill</td><td>Candidate will be able to work independently in front end VLSI/ Embedded Hardware Design with management and Supervisory</td><td>Exercise management and supervision in the context of work/study having</td><td>8</td></tr>
</table>

| | | | |
|---|---|---|---|
| **Responsibility** | responsibilities in the industry. He/she can also lead projects and teams | unpredictable changes; responsible for the work of others. | *8* |

## SECTION 3

## EVIDENCE OF NEED

**What evidence is there that the qualification is needed?**

1. Report of taskforce to suggest measures to stimulate the growth of IT, ITES, and Electronics Hardware manufacturing Industry in India – Dec 2009.

**RECOMMENDATIONS**

The Government of India would do well to foster a globally competitive industry.

The industry needs to focus on the following:

- Increased value addition
- Implementation of best practices
- Catering to the needs of domestic and global markets by creating innovative product designs and R&D
- Driving cost competitiveness

The government can catalyze this growth by the following measures:

| | | |
|---|---|---|
| 1 | Establish 'National Electronics Mission' | Establish 'National Electronics Mission' – a nodal agency for the electronics industry within DIT and with direct interface to the Prime Minister's Office (PMO). The nodal agency will help in the synchronized functioning of the industry. It will enhance the ease of doing business. |
| 2 | Promote existing clusters and create new ones | Create islands of excellence by encouraging and planning for the expansion of existing centers such as Sriprembudur, Noida, etc. and identify more locations to set up clusters to create a complete ecosystem where all the segments of the value chain are available at one location. Provide contiguous land and Infrastructure to the industry to these clusters. |
| 3 | "Made for India" Goods | Encourage products specifically designed for India. Developmental sector can benefit from biometric readers, smart meters, micro payment devices, and low cost devices. |
| 4 | Creation of a R&D fund | A fund may be created to incentivize R&D, where the government and the industry bodies are stake holders. |
| 5 | Creation of a manufacturing value addition fund | A separate fund may also be created to provide interest linked subsidy to promote value added manufacturing and create products for India. |
| 6 | Rationalization of tax structure | Stable tax structure needs to be put in place in order to encourage long term investment by the companies. |
| 7 | Promote skill development | Government needs to focus on skill development, regulations around over-time and contracts need to be flexed. |

2. Challenges and Solutions in bridging the gap of skilled human Resource (HR) in Electronics System Design and Manufacturing System. Workshop report Feb 2012.
3. Proposal to NSDC on the formation of Sector Skills Council: Electronics.
4. Employability and skills set of newly graduated Engineers in India – Andreas

Blom, Hiroshi Sakei policy research working paper (5640). World Bank.

5. Human Resource and skill Requirements in the Electronics and IT Hardware Industry.
   "Study on mapping of human resource Skill gaps in India till 2022" – NSDC / ICRA management Consulting Services Limited. (IMACS)

   **https://www.scribd.com/document/74364619/Media-Entertainment-Human-Resource-Skill-Gaps-India-2012**
6. *View Point* – Make in India – *"A Way to Boost Manufacturing and Employment opportunities" Electronics for You, June 2016.*

Evidence of qualification Requirement in the Industry – There is huge opportunities for

Physical Design Professionals in the industry – proof from Naukari.com, LinkedIn attached.

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Principal Engineer

Microchip Technology

Bangalore

• Excellent **RTL** coding and FSM **design** experience • Experience in Digital **Design** and Verification with strong **RTL** coding background... definitions, **RTL** coding, system level verification, synthesis/STA/DFT support, verification/validation support, analog **design** support...

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**RTL-2-GDSII Design**

MOBIVEIL TECHNOLOGIES INDIA PRIVATE LIMITED

KEYSKILLS > **RTL** 2 GDSII **Design** | Sub-micron Physical **design** | Physical Verification | Synopsys Flow | Clock tree **design**

Chennai

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**RTL PHY Design DDR / LPDDR / Memory controller**
MOBIVEIL TECHNOLOGIES INDIA PRIVATE LIMITED

KEYSKILLS > RTL coding | PHY Design | creating Verilog based designs

Chennai

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**FPGA with Optical Tech**

Infinite Computer Solutions India Ltd.

Bengaluru, Chennai, Gurgaon

Keyskills: Verilog, VHDL, SDH, FPGA **Design**, **RTL Design**, DWDM, Sonet, Roadm, Xilinx...

Job Description: Work location: Infinite, Chennai or Bangalore

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**Lead Application Engineer**

Cadence Design Systems

San Jose, CA, US

...: Technical Field Application **Engineer** for Cadence Digital... **ENTRY LEVEL** POSITION We offer a very aggressive.

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**Rtl Design Engineer**

Universal Hunt Private Limited

Chennai

complex IP and or ASIC blocksExperience creating Verilog based **designs** from ScratchExperience developing AXI based IPs BlocksGood...

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Senior Asic/ip Verification Engineer

Synopsys Bengaluru

SYNOPSYS® Predictable Success

Keyskills: System Verilog, Axi, C, **RTL** Coding, ASIC, Perl, Verification, Synthesis...

Job Description: Job role: The candidate will be part of the Solutions Group at our Bangalore **Design** Center, India. ...

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**ASIC (SoC) Design Engineer**

NVIDIA Santa Clara, CA

ASIC (SoC) Design Engineer. The NVIDIA System-On-Chip (SOC) group is looking for a top ASIC (SoC) Engineer with an interest in RTL integration and design as...

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**Systems** Design Engineer - **System** Level Verification

XILINX

Xilinx

San Francisco Bay Area

We are looking for a Systems Design Engineer with a strong background in software to join the System-level Test team in San Jose.

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**ASIC Verification Engineer**

Advanced Micro Devices, Inc. Orlando, FL

+ Must have ASIC design knowledge and be able to debug Verilog RTL code using simulation tools. + Must be proficient in Verilog, System Verilog, C and C++, UVM,...

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Staff Design (RTL) Engineer - Next generation memory controllers...

XILINX

Xilinx

Hyderabad Area, India

Xilinx is looking for a talented individual to join the memory interfaces design engineering group, in the position of Staff Design ...

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**What is the estimated uptake of this qualification and what is the basis of this estimate?**

Estimated uptake is 40 students / Batch with 2 Batches / Year and on the basis of market Survey /other reports and our infrastructure capabilities.

There is a huge uptake for this qualification, Proofs for the same:

1. Report of taskforce to suggest measures to stimulate the growth of IT, ITES, and Electronics Hardware manufacturing Industry in India – Dec 2009.
2. Challenges and Solutions in bridging the gap of Skilled human Resource (HR)
   in Electronics System Design and Manufacturing System.
   Workshop report Feb 2012.

**What steps were taken to ensure that the qualification(s) does/do not duplicate already existing or planned qualifications in the NSQF?**

This course structure is designed in such a way that, the qualification acquired will meet the prerequisites of higher level courses in Industrial automation system Design domain

**What arrangements are in place to monitor and review the qualification(s)? What data will be used and at what point will the qualification(s) be revised or updated?**

Based on feedback by participants, employers and based on market survey the qualification will be reviewed in every 2 years.

## SECTION 4

## EVIDENCE OF PROGRESSION

**What steps have been taken in the design of this or other qualifications to ensure that there is a clear path to other qualifications in this sector?**

This course structure is designed in such a way that, the qualification acquired will meet the prerequisites of higher level courses in this domain like Mtech in VLSI, Embedded System Design, Electronics System Design and Integrated PhD involving application research.

## SECTION 5

## EVIDENCE OF INTERNATIONAL COMPARABILITY

List any Comparisons which have been established – NIL